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Attorney Docket No.: P-6618-US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	GAT, Tal	Examiner:	LAI, VINCENT
Serial No.:	10/849,025	Group Art Unit:	2181
Filed:	May 20, 2004		
Title:	SYSTEM, DEVICE AND METHOD OF MAINTAINING IN AN ARRAY LOOP ITERATION DATA RELATED TOO BRANCH ENTRIES OF A LOOP DETECTOR		

PRE-APPEAL BRIEF AND REQUEST FOR REVIEW

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Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Pre-Appeal Brief and Request for Review is submitted together with a Notice of Appeal in response to the final Office Action dated November 2, 2006. A response was due February 2, 2007. This communication is being filed together with a Petition for one-month extension and the requisite fee. Accordingly, a response is due March 3 and the Pre-Appeal Brief and Request for Review is being timely filed.

Kindly consider the following remarks:

Remarks/Arguments begin on page 1 of this paper.

REMARKS

I. Introduction

In the final Office action, the Examiner maintained the rejection of all pending claims in the present application as follows: Claims 1, 3 – 6. 8 – 9, 11 – 13, 16 – 17 and 19 - 21 under 35 U.S.C. § 102(e), as being anticipated by Arora et al. (US. 6,629,238) (hereinafter "Arora"), claims 2, 10, 15 and 18 as being unpatentable over Arora et al. in view of Intel Itanium Processor Micro architecture Reference and claims 7 and 14 as being unpatentable over Arora et al. in view of the Inside Intel Itanium 2 Provessor. Because there were clear errors in the Examiner's rejections and/or the Examiner has omitted one or more essential elements needed for a prima facie rejection, this pre-appeal brief and request for review is suitable.

As described below, there are at least two bases for Applicants' traversal of the rejections. First, Arora does not teach every element of each independent claim. Second, Arora qualifies as prior art only under Section 102(e), as it was owned by the same assignee of the present application, Intel Corporation at the time the invention was made.

II. Discussion of Arora et al. (US. 6,629,238)

Arora discloses:

> [A] predicate predictor [that] maintains speculative loop status information. The predicate predictor uses the speculative loop status information and instruction information to predict when a predicate will be written by an associated instruction, and a value to be written for the predicate (Summary of the Invention, col. 2, lines 52-57).

Arora teaches a mechanism for predicting whether a predicate is written and a value of the predicate to be written. The Examiner contends that the loop predictor of Arora can be interpreted as a loop detector. Arora, however, does not describe any particular set of branch entries associated with its predicate predictor and certainly does not teach or suggest a separate small array to maintain, for example, the speculative counter related to a specific branch entry. Therefore, one may assume that Arora would use a standard set of branch entries that involves allocating a data storage area for both a real counter and a speculative counter for each branch entry.

Accordingly, Arora does not teach or fairly suggest, for example, "a set of branch entries to maintain data relating to a set of branches, respectively, wherein said set of branch entries includes a first number of entries; and an array able to maintain a set of iteration entries, wherein said set of iteration entries includes a second number of entries smaller than said first number of entries, wherein said loop detector is able to allocate at least one of said iteration entries to store loop iteration data relating to at least one branch entry of said set of branch entries, respectively", as recited in claims 1, 16 and 19.

III. Argument

Pending claims 1, 16 and 19 recite:

> a set of branch entries to maintain data relating to a set of branches, respectively, wherein said set of branch entries includes a first number of entries; and an array able to maintain a set of iteration entries, wherein said set of iteration entries includes a second number of entries smaller than said first number of entries, wherein said loop detector is able to allocate at least one of said iteration entries to store loop iteration data relating to at least one branch entry of said set of branch entries, respectively.

Arora discloses at column 11, lines 7 - 10:

> For the exemplary embodiment of computer system 800, memory 820 stores a program segment 824 that includes a modulo-scheduled loop.

A. Arora does not Teach Every Element of Claims 1, 5, 11, 16 and 19

In the Office Action, the Examiner contends that the element "a set of branch entries to maintain data relating to a set of branches" is discloses by Fig. 8 and col. 11, lines 7 – 10 of Arora. Column 11, lines 7 – 10 merely recites that "memory 820 stores a program segment 824 that includes a modulo-scheduled loop". The Examiner further states that "program segment 824 (854) can be made up of loop instructions". In contrast, the Examiner does not state anything regarding "a set of branch entries" since "loop instructions" or "instructions for a modulo-scheduled loop", as described in Arora are in no way analogous to "entries to maintain data relating to a set of branches".

As explained in the subject application with reference to Fig. 1, the entries may correspond to the several least significant bits of an address of a branch and may include data storage space for storing a tag, a real counter and a max counter (see par. [0010]).

In the Office Action, the Examiner contends that the element "an array able to maintain a set of iterations entries, wherein said set of iteration entries includes a second number of entries smaller that said first number of entries" is also disclosed by Fig. 8 and col. 11, lines 7 – 10 of Arora. The Examiner further states that "memory 820 (850) can be used to store loops" and that "pictorially, the program segment is smaller that the memory" (emphasis added). The Examiner further contends that "since the program segment is meant to fit in memory, it is inherently smaller than memory". These conjectures and speculations are simply unsupported by the Arora reference.

Applicant respectfully asserts that memory 850 of Arora is not analogous to "an array able to maintain a set of iterations". Paragraph [0011] of the subject application teaches a loop detector that may include one or more arrays 20, for example, a fully associative array with four array entries 18. Array entries include data storage that may store a counter such as, for example, a speculative counter.

Further, even in light of the Examiner's erroneous interpretation of the terms "set of branch entries" as being program segment 854 and "set of iteration entries" as being memory 850, it does not appear pictorially that the second number associated with the iteration entries is smaller than the first number associated with the branch entries; if anything can be surmised from the block diagram of Fig. 8 it is the exact opposite.

In the Office Action, the Examiner contended that the element "said loop detector is able to allocate at least one of said iteration entries to store loop iteration data relating to at least one branch entry" is also disclosed by Fig. 8 and col. 11, lines 7 – 10 of Arora. The Examiner further stated that "saving to memory means that loop detector will store data". As explained above, the recitation is not related to "store loop iteration data relating to at least one branch entry".

Similar arguments can be made with respect to claims 5 and 11. Thus, it is respectfully requested that the rejection of independent claims 1, 5, 11, 16, and 19 and its dependent claims under 35 U.S.C. § 102(e) be withdrawn.

B. The Arora Reference does not qualify as prior art under 35 U.S.C. § 103

According to 35 U.S.C. § 103(c) "[s]ubject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person."

As cited by the Examiner in the Office action, the Arora reference qualifies as prior art under Section 102(e). The Arora reference, however, was owned by the same assignee of the present application, Intel Corporation at the time the invention was made. Therefore, Arora cannot be cited against the present application under 35 U.S.C § 103(a). Accordingly, Applicants respectfully assert that the rejection under 35 U.S.C. § 103(a) over Arora et al. in view of Intel Itanium Processor Micro architecture Reference or Inside Intel Itanium 2 Professor should be withdrawn.

Thus, it is respectfully requested that the rejection of claims 2, 7, 10, 14, 15, and 18 under 35 U.S.C. § 103(a) is improper and should be withdrawn. In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Respectfully submitted,

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